CLAIMS

1. A switching circuit comprising an input operable to receive a DC signal of $+V_S$, an output, first and second switches operable in response to first and second switching signals to be switched between on and off states such that switching between various combinations of on and off states produces an electrical signal at the output with voltage pulses at levels of $+V_S$, 0V and $-V_S$ and a voltage sensor for producing a signal indicative of a voltage offset in the switching circuit.

2. A switching circuit according to claim 1, wherein the voltage sensor is arranged to measure fluctuations in the DC signal.

3. A switching circuit according to claim 1, wherein the voltage sensor is arranged to produce a signal indicative of a predicted value of the DC signal.

4. A switching circuit according to claim 3, wherein the voltage sensor includes a finite impulse response filter arranged to measure the DC signal.

5. A switching circuit according to any of claims 1 to 4, wherein the voltage sensor is operable to produce a signal indicative of a voltage drop across a diode and/or transistor in the switching circuit.

6. A switching circuit according to claim 5, wherein the voltage sensor is arranged to measure the current flowing through the output.

7. A switching circuit according to claim 6, wherein the voltage sensor is operable to produce a signal indicative of a voltage drop across a diode and/or transistor of the switching circuit with reference to a measurement of the current flowing through the output and a value of the resistance of the diode and/or transistor.

8. A switching circuit according to any of claims 1 to 7, comprising a bridge circuit having an input that receives a DC signal of voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output.

9. A switching circuit according to claim 8, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

10. A switching circuit according to claim 8 or claim 9, wherein the first and second switches are transistors.

11. A switching circuit according to any of claims 8 to 10, wherein an electromagnet is connected across the output of the bridge circuit.

12. A switching circuit according to any of claims 1 to 11, further comprising a noise shaper operable to noise-shape the first and second switching signals.

13. A method of operating a switching circuit comprising an input that receives a DC signal of voltage $+V_S$, an output and first and second switches, the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period;

(b) generating first and second switching signals with reference to the voltage demand signal and with reference to a voltage offset in the switching circuit; and

(c) applying the first and second switching signals to the first and second switches respectively during the period;

wherein the switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches producing an electrical signal at the output with voltage pulses at levels of $+V_S$, 0V and $-V_S$,

the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the output during the period is substantially equal to the desired voltage.

14. The method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC signal such that the at least one first or second switching signal compensates for fluctuations in the DC supply.

15. The method of claim 14, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply.

16. The method of claim 15, wherein the voltage signal is passed through a finite impulse response filter.

17. The method of any of claims 13 to 16, wherein at least one of the first and second switching signals is generated to compensate for a voltage drop across a diode and/or transistor in the switching circuit.

18. The method of claim 17, wherein the at least one first or second switching signal is generated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode or transistor.

19. The method of any of claims 13 to 18, wherein at least one of the first or second switching signals is generated with reference to a measure of a voltage offset caused by slow response times in the first or second switch.

20. The method of any of claims 13 to 19, wherein the switching circuit comprises a bridge circuit having an input that receives a DC signal of voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output.

21. The method of claim 20, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

22. The method of claim 20 or claim 21, wherein the first and second switches are transistors and the method comprises the step of switching the transistors between on and off states corresponding to substantially maximum and substantially minimum current flow respectively through the transistors.

23. The method of any of claims 13 to 22 comprising the step of generating pulsed first and second switching signals.

24. The method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently.

25. The method of claim 23 or 24 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period.

26. The method of claim 25 comprising the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period.

27. The method of claim 26 comprising the step of generating the first and second switching signals according to the rule that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive pulses.

28. The method of any of claims 23 to 27 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme.

29. The method of any of claims 23 to 28 comprising the step of noise shaping the first and second switching signals.

30. The method of any of claims 13 to 29 comprising the step of receiving a current demand signal indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current.

31. The method of claim 30, wherein the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output.

32. The method of claim 30 or claim 31 further comprising the step of generating the voltage demand signal with reference to a current signal indicative of the current flowing through the output.

33. A computer program comprising program code means for performing the method steps of any of claims 13 to 32 when the program is run on a computer and/or other processing means associated with the switching circuit.

34. A computer program product comprising program code means stored on a computer readable medium for performing the method steps of any of claims 13 to 22 when the program is run on a computer and/or other processing means associated with the switching circuit.

35. A switching circuit according to any of claims 1 to 12, further comprising processing means programmed to perform the method steps of any of claims 13 to 32.

36. A switching circuit substantially as hereinbefore described with reference to any of Figures 1 to 6.

37. A method of operating a switching circuit substantially as hereinbefore described with reference to any of Figures 1 to 6.